A SOI FinFET device model based on Verilog-A for proton-irradiation influence analysis

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***Abstract*—In this work, a simple methodology is proposed to analyze FinFET devices behavior. Since this component does not have a precise first order analytical model to be collected from physical simulation programs, it is proposed to use a method called lookup table in Verilog-A. This method consists of a detailed experimental characterization of the device in order to obtain its behavior and then feed the lookup table with the data and its interpolation, to be used in simulations. The benefits of using this model over compact models is that it is used the device's experimental response to simulations, as well as it is not needed to use complex physical models and wait the device technology consolidation to simulate the device performance within a circuit, reducing the number of steps required. This method can be validated comparing the accuracy between the experimental data with the obtained simulated one. Using the proposed method, FinFET devices of different fin widths were analyzed, before and after proton-irradiation and all designed curves show a great compliance between experimental and simulated data and expected behavior from the studied devices, permitting further analysis of the components inside a complex circuit.**

Keywords—FinFET, proton-irradiation, Verilog-A

I. INTRODUCTION

To be able to build systems using a semiconductor's made device, whichever device chosen, it is common to use simulation programs in research stage. It enables primarily the reduction of costs, once you can predict the final result before the construction of a prototype. These simulation programs can predict the electrical behavior of the device by its physical conditions and bias applied [1].

Nonetheless, with the advance of the used technology to build semiconductors' devices, the new structures are more complex than the conventional metal-oxide-semiconductor (MOS) technology, which creates more complexity for the simulation programs to predict its behavior since they do not have an accurate first order analytic model [1]-[3]. Beyond that, the behavioral prediction might be even less reliable when it comes to the proposal of exposing devices to radiation-harsh environments.

Due to the difference between the simulated and measured devices behavior promoted by the physical model, it is important to develop a method that makes it possible to simulate devices within a circuit based on its measured performance, instead of the simulated one. It excludes the need of a physical model and creates a more reliable method of simulation.

This work proposes the simulation using Verilog-A, software which allows to simulate circuits based on the real device behavior from its previous measurements using the lookup table method [4].

The device considered in this work will be the triple-gate SOI MOSFET, also called FinFET, which does not have an accurate first order analytic model as well as many other transistor devices [5]. This will also allow simulating and comparing the behavior of the FinFET between before and after exposure to radiation-harsh environments.

It is known that the Silicon-on-Insulator (SOI) technology has proven to have a superior transient performance on operating in radiation-harsh environments, when in comparison to bulk transistors. This improvement is due to the thin active silicon region that provides a better electrostatic coupling and the existence of the buried oxide beneath the channel that isolates the transistor active area from the substrate [5]-[7].

Even though the SOI technology provides significant immunity to the radiation effects when compared to bulk transistors, the radiation effect still have to be considered because the trapped charges in the buried oxide (BOX) affect the transistor characteristics [5]-[7].

Additionally, it is important to notice that when it comes to downscaling of devices, the SOI technology is a suitable option over bulk transistors, since it promotes a better control of the short-channel effects (SCE) [5].

Although studies on using Verilog-A for FinFET's circuit simulation [3][8] and the proton-irradiation effect on FinFET devices [9] have already been made, the investigation of the lookup table method using experimental data for pre and post radiation FinFET devices should be validated to allow further investigation of complex circuits using irradiated FinFET devices. This work aims to initiate the studies on FinFETs simulation regarding proton-irradiation effect using Verilog-A.

II. DEVICE CHARACTERISTICS

The studied devices are n-type triple-gate SOI MOSFETs (FinFETs) fabricated in imec, Belgium. They were processed on SOI substrates with a thick buried oxide (t_{BOX}) of 150 nm. The fin height (h_{FIN}) is 65 nm and the channel length (L) is 150 nm, both constant, and three fin widths (W_{FIN}) were compared: 20 nm, 120 nm and 870 nm. Each transistor has 5 fins in parallel. The gate dielectric of the devices consists of 2 nm HfSiON on 1 nm SiO_2 interfacial layer, resulting in an Equivalent Oxide Thickness (EOT) of 1.5 nm. The gate is 10 nm TiN covered by 100 nm poli-Si.

The proton irradiation has been performed at the Cyclone facility in Louvain-la-Neuve (Belgium). The beam energy is 60 MeV up to fluence of 10^{12} p/cm^2. No bias was applied during the irradiation and all the devices are unpackaged.

The measurements were performed at room temperature, using a Keysight Agilent B1500A semiconductor device analyzer.

Figure 1 shows a schematic view of a triple-gate SOI MOSFET (FinFET) structure.

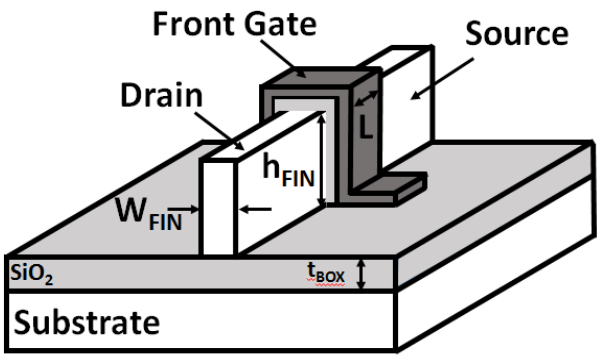

Fig. 1. Triple-gate SOI MOSFET (FinFET) structure.

III. Experimental Device Modelling

In order to acquire a reliable experimental model, all the measurements were performed to obtain the drain current response for both front gate voltage and drain voltage bias, with small steps.

After obtained, the data can be used to define the device behavior for all the proposed situations; in other words, it will provide the current response for each voltage condition the device may acquire in a circuit, which can make it possible to simulate the device within a circuit, in the future.

The acquired data were later stored in a table file to be accessed by the Verilog-A model, using a method called lookup table model [4]. This model is reliable because it uses the experimental device behavior once measured, rather than analytical models. Moreover, the method provides both interpolation and extrapolation of the experimental data once obtained. These features are important to provide stable and predictable data from simulated behaviors, avoiding deviations and also accessing extended values for other bias conditions.

To validate the lookup table model behavior, it was used the Verilog-A model on the Cadence Virtuoso schematic capture environment. The simulations were performed at the Cadence Analog Design Environment. To be able to reproduce this simulation, first it was designed a new component and using the Verilog-A code simulation and the lookup table is linked to the device operation, where the gate and the drain voltages are the inputs and drain current is the output. When, during the simulation, a gate and drain voltages are selected, the lookup table must provide a drain current value by exact, interpolation or extrapolation values.

For all the measured and simulated data, the back gate and the source are connected to the ground. The detailed measurements were made varying the front gate and drain bias, as follow: V_{GF} from -0.5 V to 1.5 V for each V_{DS} (from 0V to 1.5V with steps of 0.05V), to design I_{DS} x V_{GF} graphics. The output characteristics were also measured in order to validate the data from the first table and design I_{DS} x V_D graphics.

Figure 2 shows the test-bench designed to validate the lookup table model. It consists basically of the N-FinFET and the voltage sources, connected to the front gate, back gate, drain and source terminals.

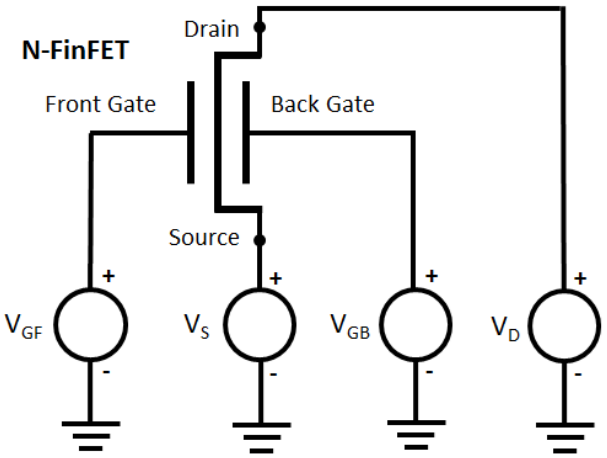

Fig. 2. Test-bench designed to validate the lookup table model.

Figure 3 shows the drain current (I_{DS}) as a function of the front gate voltage (V_{GF}) for different fin widths before the radiation, for measured (symbols) and simulated (lines) data. From figure 3, it is possible to notice that the simulation values accurately fit the experimental data, for both linear and logarithm scale. It can also be noticed that the model is able to faithfully reproduce the behavior of the short channel FinFETs which suffer from short-channel effects (SCE).

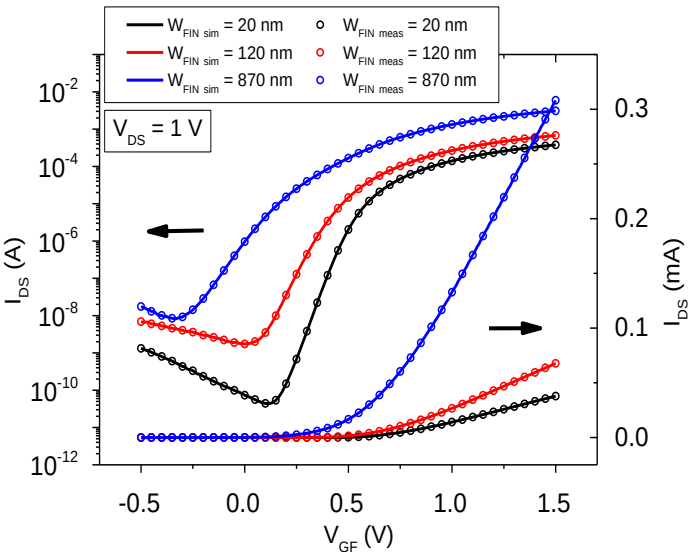

Fig. 3. Simulated (lines) and measured (points) of the drain current (I_{DS}) as a function of the front gate voltage (V_{GF}) for different fin widths (W_{FIN}) before the radiation.

Figure 4 shows the drain current (I_{DS}) as a function of the drain voltage (V_{DS}), also comparing the measured and the simulated data for model validation.

From the figure 4 it is possible to verify that since the first measured data inserted in the lookup table have small steps, it is possible to simulate the devices behavior even for another bias variation (V_{DS} instead of V_{GF}) and still achieve a

good agreement. Both figures 3 and 4 prove that it is reliable to use the lookup table model using Verilog-A to simulate the real device behavior using this method.

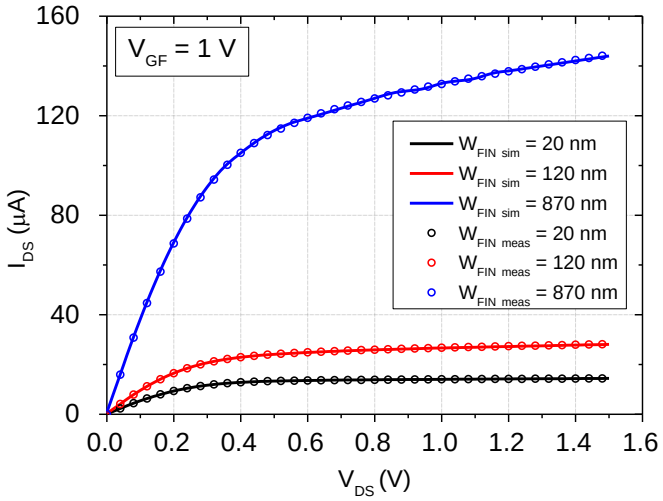

Fig. 4. Simulated (lines) and measured (points) of the drain current (I_{DS}) as a function of the drain voltage (V_{DS}) for different fin widths (W_{FIN}), pre-radiation.

Since the model efficiently fits for pre-radiation devices, some measurements for nFINFETs were done after the devices were exposed to radiation and the same comparisons and analysis were performed.

Figure 5 shows only the simulated curves of the drain current (I_{DS}) as a function of the front gate voltage (V_{GF}), for drain voltages (V_{DS}) of 50 mV and 1.5 V and fin widths (W_{FIN}) of 20 nm, 120 nm e 870 nm, comparing before and after radiation. It was not necessary to add the measure data in the graph because both curves fitted, since they came from the same lookup table.

From the figure 5 it is possible to notice that proton irradiation causes degradation on subthreshold swing (SS), except on the narrowest studied device. The reason for it to occur is that a radiation induces positive charges in the buried oxide and resulting in a threshold voltage at the back interface (V_{th2}) reduction. As a consequence, the current of the back interface increases, degrading the subthreshold swing. Narrow devices are almost not affected because the radiation has no significant influence, due a higher coupling between gates, which promotes a shield from oxide trap charges. With the increase of the fin width, the radiation influence on the SS behavior increases as well [9][10].

Figure 6 shows both the simulated and measured curves of the drain current (I_{DS}) as a function of the drain voltage (V_{DS}) for front gate voltages (V_{GF}) of 1 V and 1.5 V and fin widths (W_{FIN}) of 20 nm, 120 nm e 870 nm, comparing before and after radiation. This curve contains additionally the measured data in order to validate the model also for radiated devices.

From figure 6 is possible to notice that in the saturation region, the irradiation of devices causes an increase of the drain current. As said before, narrow devices are almost not affected because the radiation has no significant influence. The drain current raise can be explained by the drain current dependence with overdrive voltage ($V_{GT} = V_{GF}-V_T$), that in turns is increased with radiation due to the V_T reduction [6].

Since the graphs are plotted for the same V_{GS}, is spite of V_{GT}, the I_{DS} curves post-radiation are a little bit higher than the pre-radiated ones.

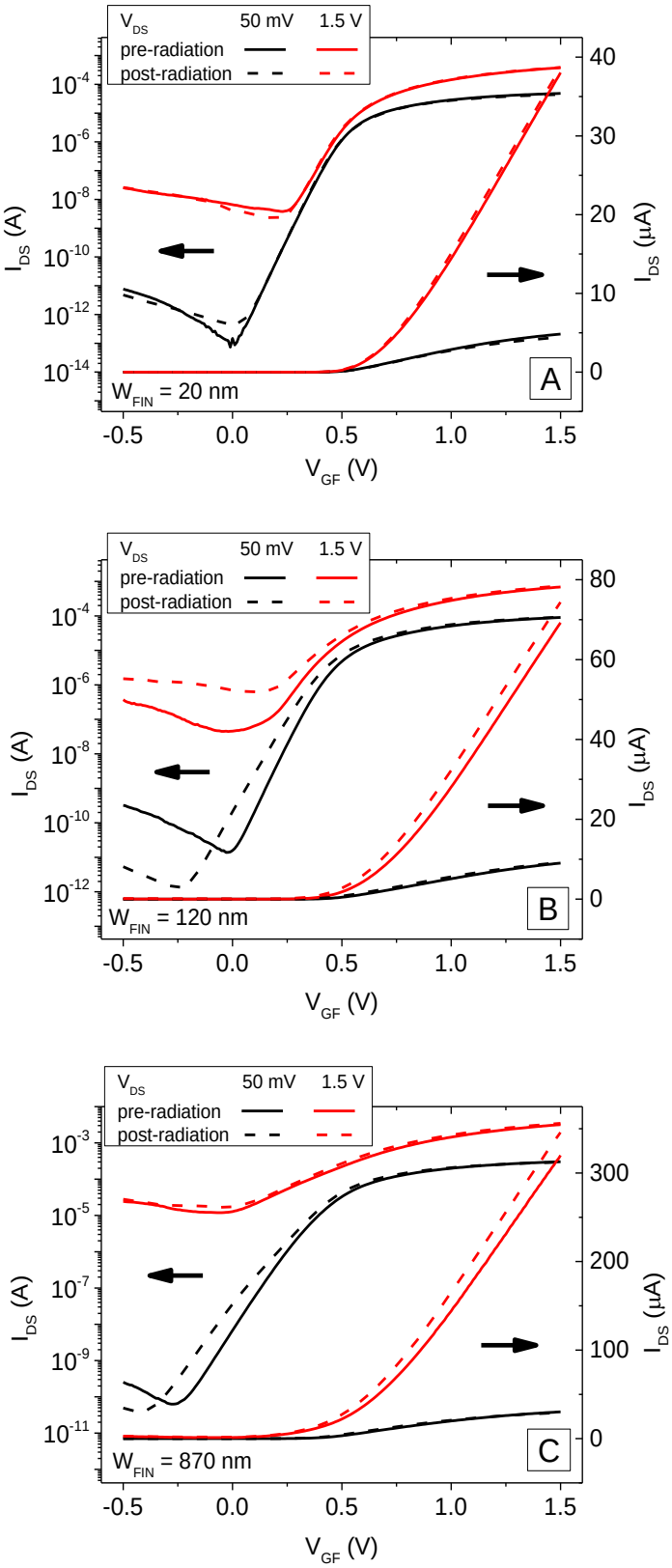

Fig. 5. Simulated curves of the drain current (I_{DS}) as a function of the front gate voltage (V_{GF}) for drain voltages (V_{DS}) of 50 mV and 1.5V and 3 different fin widths (W_{FIN}) 20 nm (A), 120 nm (B) e 870 nm (C), pre and post radiation.

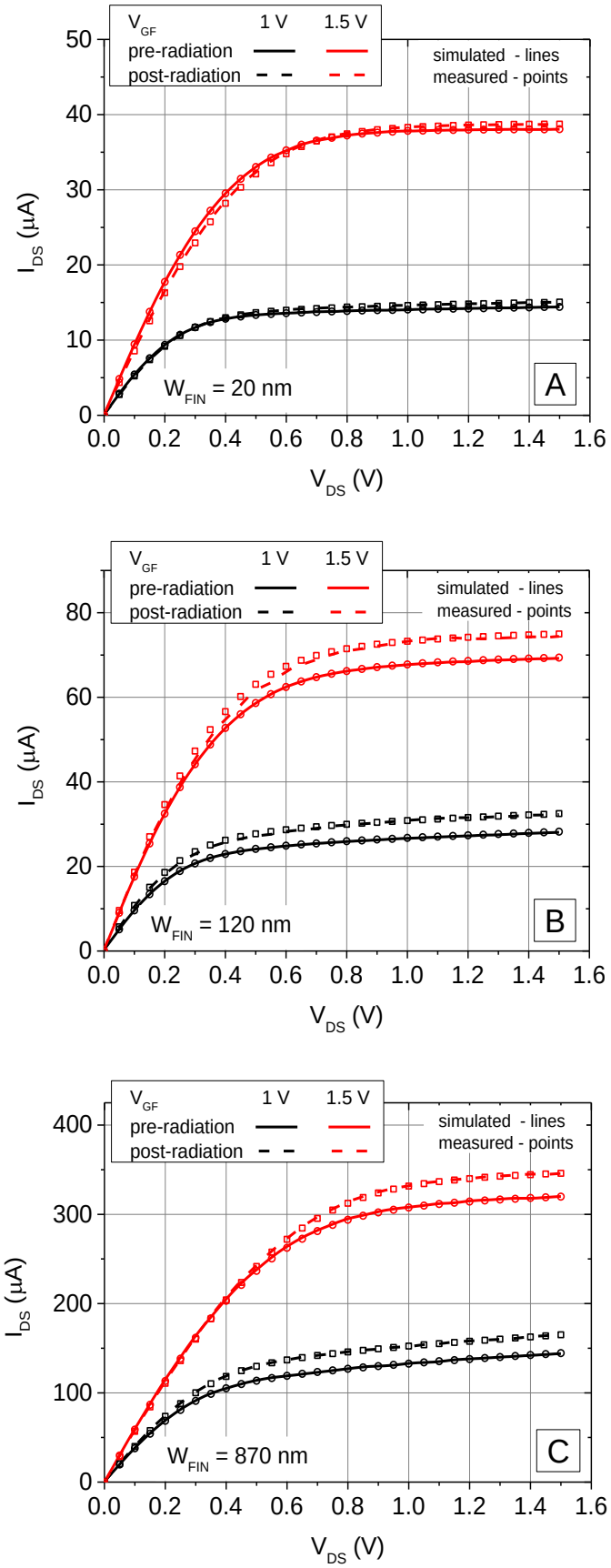

Fig. 6. Simulated (lines) and measured (points) of the drain current (I_{DS}) as a function of the drain voltage (V_{DS}) for front gate voltages (V_{GF}) of 1 V and 1.5V and 3 different fin widths (W_{FIN}) 20 nm (A), 120 nm (B) e 870 nm (C), pre and post radiation.

IV. Conclusion

The proposal of this work is to suggest a new approach for the simulation of FinFET devices based on the lookup table model using Verilog-A approach. The process consisted of a characterization of devices for chosen bias combination with small steps and construction of a table to be accessed by the simulation. This allows the simulation program to access the table and predicts the behavior of components using truly experimental data.

First, to affirm that this method is reliable, it has been made a comparison between measured data and the simulated data obtained. Since both curves fitted with a great agreement, this method has been proven to be reliable.

Second, analyzing the measured and simulated curves regarding the FinFET behavior and the radiation matter, it is possible to certify that, based on previous works, both data have proven to be consistent as expected. So, it is possible to conclude that the experimental data obtained are reliable and could be used to simulate the component behavior within a circuit, even in a complex one. Further studies intend to demonstrate the application of the same method presented to create and analyze complex circuits using FinFETs.

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